ED STATES PATENT AND TRADEMARK OFFICE

Applicant:

Cheng-Lien Chiang

Assignee:

Bridge Semiconductor Corporation

Title:

METHOD OF MAKING A SEMICONDUCTOR PACKAGE

DEVICE THAT INCLUDES A CONDUCTIVE TRACE WITH

RECESSED AND NON-RECESSED PORTIONS

Serial No.:

10/059,686

Filed:

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Examiner:

Zarneke, D.

Group Art Unit:

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BDG005-1

COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, VA 22313

TRANSMITTAL OF FORMAL DRAWINGS

Attached please find the formal drawings (29 sheets) for this application.

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail

EU267708508US in an envelope addressed to: Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 15, 2003.

David M. Sigmond

12,15,03

Attorney for Applicant

Date of Signature

Respectfully submitted,

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